ABSTRACT OF THE DISCLOSURE

A method and apparatus for testing a memory at speed. A test and repair wrapper integrated with a memory instance is operable to receive test information scanned in from a built-in self-test and repair (BISTR) processor. Logic circuitry associated with the test and repair wrapper is operable to generate address, data and command signals based on the scanned test information, wherein the signals are used for effectuating one or more tests with respect to the memory instance.